IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amendeed) A clock and data recovery unit for recovering a received serial data bit stream having:

(a) phase adjustment means for adjustment of a sampling time in the center of a unit interval of the received data bit stream, wherein the phase adjustment means comprises:

(a1) means for generating equidistant reference phase signals;

(a2) a phase interpolation unit which rotates the generated reference phase signals with a predetermined granularity in response to a rotation control signal;

(a3) an oversampling unit for oversampling the received data bit stream with the rotated reference phase signals according to a predetermined oversampling rate;

(a4) a serial-to-parallel-conversion unit which converts the oversampled data bit stream into a deserialized data bit stream with a predetermined decimation factor;

(a5) a binary phase detection unit for detecting an average phase difference between the received serial data bit stream and the rotated reference phase signal by adjusting a phase detector gain depending on an[[the]] actual data density of the deserialized data bit stream such that the variation of the average phase detection gain is minimized; and

(a6) a loop filter for filtering the detected average phase difference to generate the rotation control signal for the phase interpolation unit;

(b) data recognition means for recovery of the received data bit stream which includes a number of parallel data recognition FIR-Filters, wherein each data recognition FIR-Filter comprises:

(b1) a weighting unit for weighting data samples of the deserialized data stream around the sampling time adjusted by the phase adjustment means;

(b2) a summing unit for summing up the weighted data samples; and

(b3) a comparator unit for comparing the summed up data samples with a threshold value to detect the logic value of a data bit within the received serial data bit stream.

2. (Currently Amended) The clock and data recovery unit according to claim 1 wherein the binary phase detection unit comprises:

means for detecting the actual data density of the ~~parallised~~ deserialized data bit stream; and

means for adjusting the phase detector gain depending on the detected actual data density.

3. (Original) The clock and data recovery unit according to claim 2 wherein the means for detecting the actual data density comprises a plurality of EXOR gates,

wherein each EXOR gate compares two neighboring data samples generated by the oversampling unit to decide whether a data transition has occurred.

4. (Previously Presented) The clock and data recovery unit according to claim 3 wherein the means for detecting the actual data density further comprises summation means for accumulating the number of transitions detected by the EXOR gates.

5. (Previously Presented) The clock and data recovery unit according to claim 4 wherein the means for adjusting the phase detector gain calculates the phase detector gain by multiplying the accumulated number of transitions with a multiplication factor.

6. (Previously Presented) The clock and data recovery unit according to claim 5 wherein the multiplication factor is increased when the detected number of transitions is decreased.

7. (Previously Presented) The clock and data recovery unit according to claim 3 wherein the number of EXOR gates for detection of the actual data density is given by the product of the decimation factor of the serial-to-parallel-conversion unit and the oversampling rate of the oversampling unit.

8. (Previously Presented) The clock and data recovery unit according to claim 1 wherein the decimation factor of the serial to parallel conversion unit is eight.

9. (Previously Presented) The clock and data recovery unit according to claim 1 wherein the oversampling rate of the oversampling unit is four.

10. (Currently Amended) The clock and data recovery unit according to claim 1 wherein a[[the]] data transmission rate of the serial data bit stream is more than one Gigabit per second.

11. (Original) The clock and data recovery unit according to claim 1 wherein the weighting unit of the data recognition means comprises signal amplifiers, wherein each signal amplifier amplifies a respective data sample with a programmable gain.

12. (Original) The clock and data recovery unit according to claim 1 wherein the data recognition FIR-Filters of the data recognition means are connected to a FIFO-memory.

13. (Previously Presented) The clock and data recovery unit according to claim 1 wherein the number of data recognition FIR-Filters corresponds to the decimation factor of the serial-to-parallel-conversion unit.

14. (Previously Presented) The clock and data recovery unit according to claim 1 wherein the oversampling unit comprises a predetermined number of clock triggered sampling elements.

15. (Original) The clock and data recovery unit according to claim 14 wherein the sampling elements are D-Flip-Flops.

16. (Original) The clock and data recovery unit according to claim 14 wherein the sampling elements are D-Latches.

17. (Previously Presented) The clock and data recovery unit according to claim 14 wherein each sampling element is clocked by a corresponding rotated reference phase signal generated by the phase interpolation unit.

18. (Currently Amended) The clock and data recovery unit according to claim 17, wherein the phase interpolation unit comprises a phase interpolator and a multiplexer for rotating the reference phase signals in response to the rotation control signal.

19. (Currently Amended) The clock and data recovery unit according to claim 1 wherein a[[the]] delay locked loop receives a reference clock signal from a reference clock generator.

20. (Previously Presented) The clock and data recovery unit according to claim 19 wherein the reference clock generator is a phase locked loop.

21. (Original) The clock and data recovery unit according to claim 1 wherein the loop filter has a PID-characteristic.

22. (Original) The clock and data recovery unit according to claim 1 wherein the loop filter is programmable.

23. (Original) The clock and data recovery unit according to claim 1 wherein a lock detection unit is provided which detects whether the clock and data recovery unit is locked to the received serial data bit stream.

24. (Currently Amended) The clock and data recovery unit according to claim 1 wherein a transition loss ~~the~~ detection unit is provided which detects when the serial data bit stream has stopped.

25. (Original) The clock and data recovery unit according to claim 1 wherein the phase adjustment means and the data recognition means are integrated in a digital control unit.

26. (Currently Amended) The clock and data recovery unit according to claim 25 wherein the digital control unit further includes a[[the]] lock detection unit and a[[the]] transition loss detection unit.

27. (Currently Amended) The clock and data recovery unit according to claim 24 wherein a multiplexer for rotating the reference phase signal in response to the rotation control signal is integrated in a[[said]] digital control unit.

28. (Currently Amended) The clock and data recovery unit according to claim 1 wherein the equidistant reference phase signals generated by a[[the]] delay locked loop have a phase difference $\Delta\varphi$ of 45° to define eight phase segments.

29. (Original) The clock and data recovery unit according to claim 28 wherein the phase interpolator interpolates phase signals in each phase segment on the basis of the equidistant reference phase signals.

30. (Previously Presented) The clock and data recovery unit according to claim 1 wherein the means for generating equidistant reference phase signals are formed by a delay locked loop.

31. (Currently Amended) Method for clock and data recovery of a received serial data bit stream comprising the following steps:

(a) adjusting a sampling time in the center of a unit interval of a received data bit comprising the following substeps:

(a1) rotating generated reference phase signals in response to a rotation control signal;

(a2) oversampling the received data bit stream with the rotated reference phase signals;

(a3) converting an[[the]] oversampled data bit stream into a deserialized data stream;

(a4) detecting an average phase difference between the received serial data bit stream and the rotated phase signals by adjusting a phase detector gain ~~(PDG)~~ depending on a[[the]] data density of the deserialized data stream to minimize the variation of an[[the]] average phase detector gain;

(a5) filtering the detected phase difference to generate the rotation control signal.

(b) recovering the received data bit stream comprising the following substeps:

(b1) weighting data samples of the ~~parallised~~ deserialized data stream around the adjusted sampling time;

(b2) summing up the weighted data samples;

(b3) comparing the summed up weighted data samples with a threshold value to detect the logic value of a data bit within the serial data bit stream.